
MSM66101

OLMS-66K Series 16-Bit Microcontroller

GENERAL DESCRIPTION

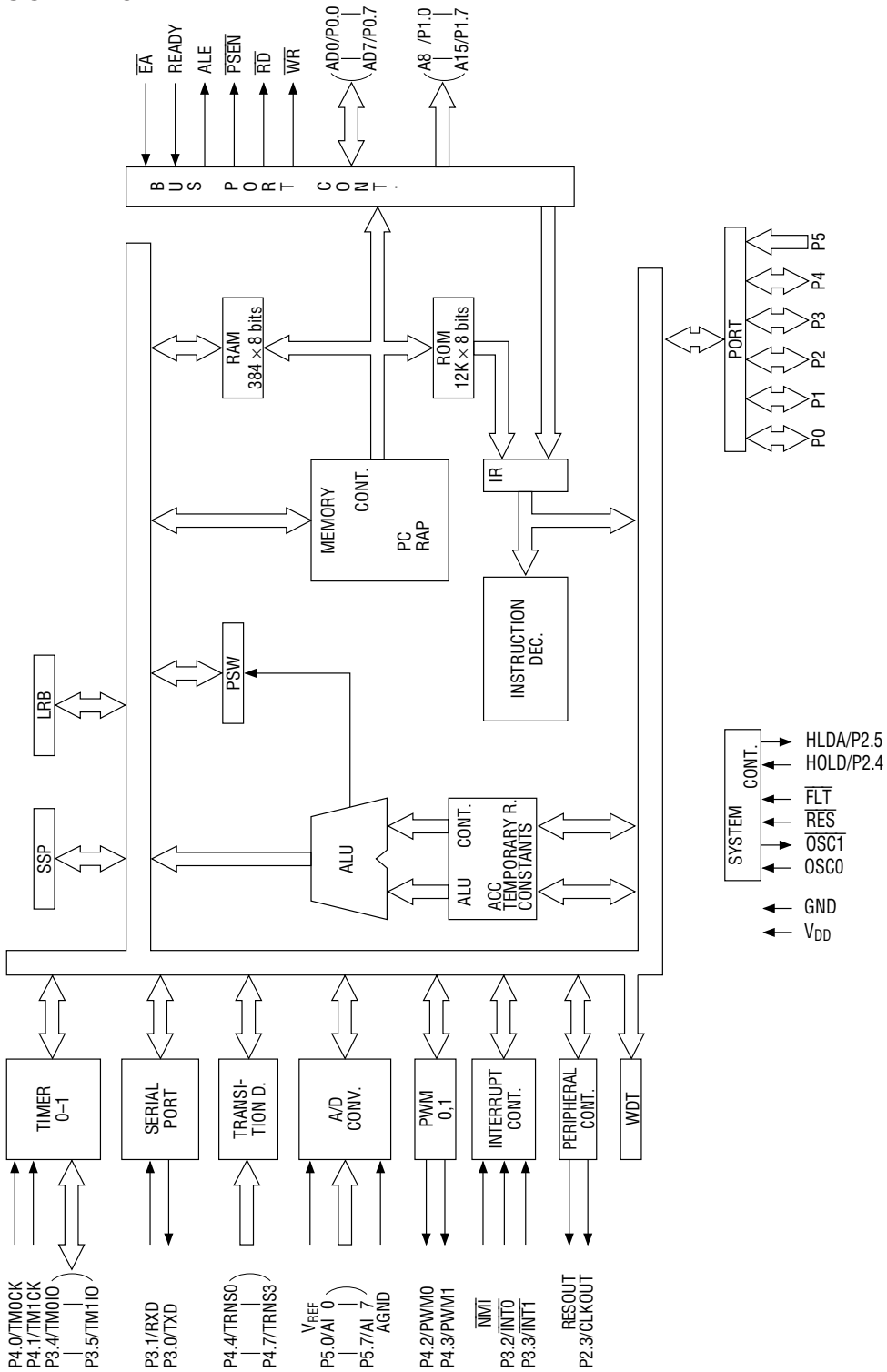
The MSM66101 is a high performance microcontroller that employs OKI original nX-8/100 CPU core. This chip includes a 16-bit CPU, ROM, RAM, I/O ports, multifunction 16-bit timers, 10-bit A/D converter, serial I/O port, and pulse width modulator (PWM).

FEATURES

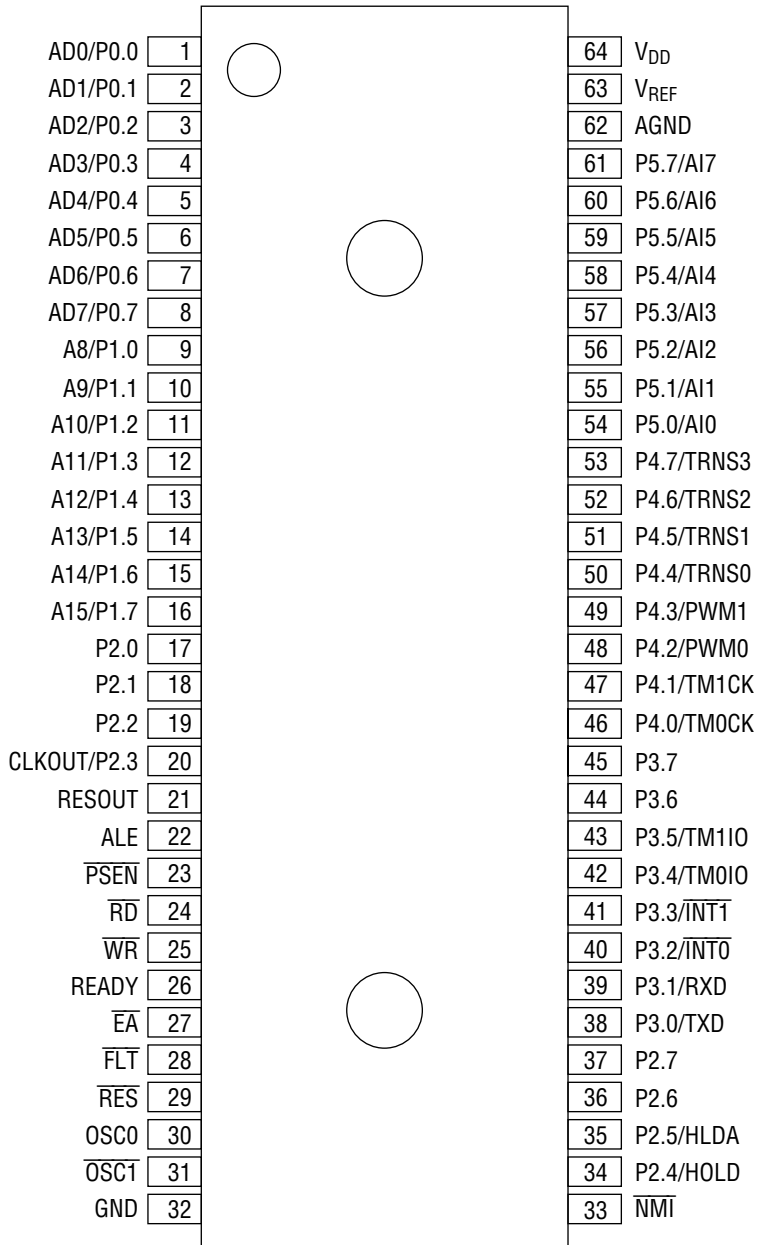
- 64K address space for program memory : Internal ROM : 12K bytes
- 64K address space for data memory : Internal RAM : 384 bytes
- High-speed execution
 - Minimum cycle for instruction : 400ns @ 10MHz
- Powerful instruction set : Instruction set superior in orthogonal matrix
 - 8/16-bit data transfer instructions
 - 8/16-bit arithmetic instructions
 - Multiplication and division operation instructions
 - Bit manipulation instructions
 - Bit logic instructions
 - ROM table reference instructions
- Abundant addressing modes : Register addressing
 - Page addressing
 - Pointing register indirect addressing
 - Stack addressing
 - Immediate value addressing
- I/O port
 - Input-output port : 5 ports × 8 bits
(Each bit can be assigned to input or output)
 - Input port : 1 port × 8 bits
- Built-in multifunctional 16-bit timer : 2
 - Following 4 modes can be set for each timer : Auto-reload timer mode
 - Clock output mode
 - Capture register mode
 - Real time output mode
- Serial port : 1 channel (UART mode with baud rate generator)
- 12-bit pulse width modulator : 2
- Watchdog timer
- Transition detector : 4
- 10-bit A/D converter : 8 channels
- Interrupts
 - Nonmaskable : 1
 - Maskable : Internal 10/external 2
- Stand-by function
 - STOP mode : Software clock stop mode
 - HALT mode : Software CPU stop mode
 - HOLD mode : Hardware CPU stop mode

- Package options:
 - 64-pin plastic shrink DIP (SDIP64-P-750-1.78) : (Product name: MSM66101-xxxSS)
 - 64-pin plastic QFP (QFP64-P-1414-0.80-BK) : (Product name: MSM66101-xxxGS-BK)
 - 68-pin plastic QFJ (PLCC) (QFJ68-P-S950-1.27) : (Product name: MSM66101-xxxJS)
 - 64-pin ceramic piggyback (ADIP64-C-750-1.78) : (Product name: MSM66G101VS)
- * The piggyback type is used only for engineering samples.
xxx indicates the code number.

BLOCK DIAGRAM

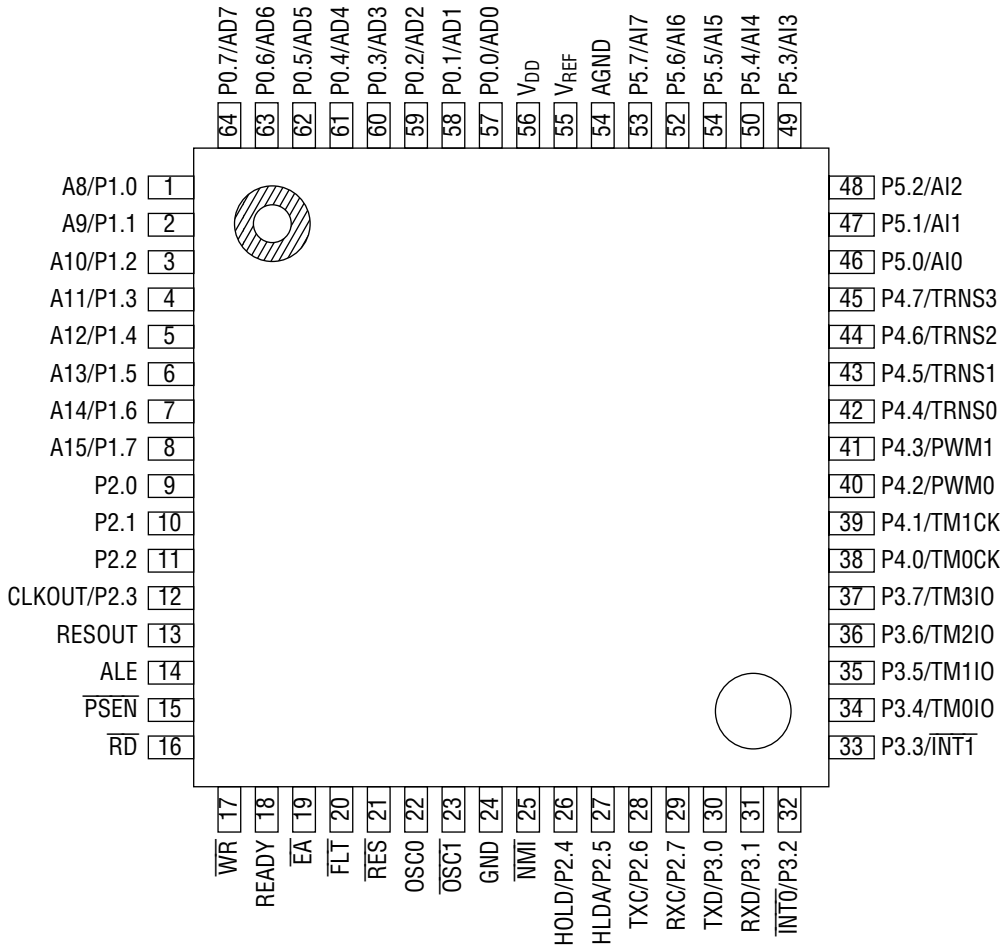


PIN CONFIGURATION (TOP VIEW)



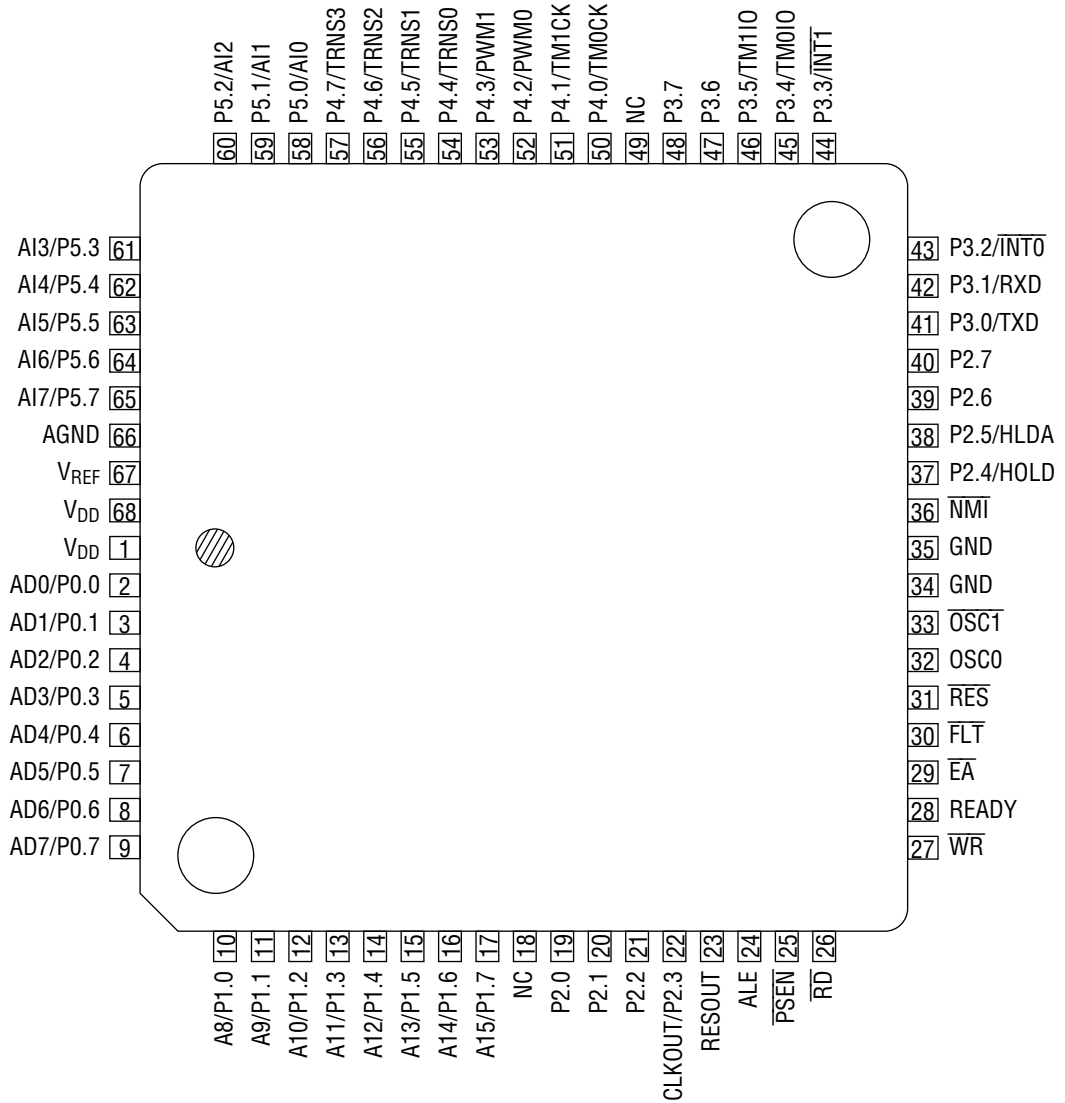
64-Pin Plastic Shrink DIP

PIN CONFIGURATION (TOP VIEW) (Continued)



64-Pin Plastic QFP

PIN CONFIGURATION (TOP VIEW) (Continued)



NC: No-connection pin

68-Pin Plastic QFJ (PLCC)

PIN DESCRIPTIONS

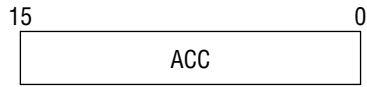
Symbol	Type	Description
P0.0–P0.7/ AD0–AD7	I/O	P0: 8-bit input-output port. Each bit can be assigned to input or output. AD: Outputs the lower 8 bits of program counter during external program memory fetch, and receives the addressed instruction under the control of PSEN. Also outputs the address and outputs or inputs data during an external data memory access instruction under the control of ALE, RD, and WR.
P1.0–P1.7/ A8–A15	I/O	P1: 8-bit input-output port. Each bit can be assigned to input or output. A: Outputs the upper 8 bits of program counter (PC _{8–15}) during external program memory fetch. Also this pin outputs the upper 8 bits of address during external data memory access instructions.
P2.0–P2.2 P2.3/CLKOUT P2.4/HOLD P2.5/HLDA P2.6 P2.7	I/O	P2: 8-bit input-output port. Each bit can be assigned to input or output. CLKOUT: Output pin for supplying a clock to peripheral circuits. Output frequency range is equal to or twice the system clock. HOLD: Input pin to request the CPU to enter the hardware power-down state. HLDA: HOLD ACKNOWLEDGE: the HLDA signal appears in response to the HOLD signal and indicates that the CPU has entered the power-down state.
P3.0/TxD P3.1/RxD P3.2/ $\overline{\text{INT0}}$ P3.3/ $\overline{\text{INT1}}$ P3.4/TM0IO P3.5/TM1IO P3.6 P3.7	I/O	P3: 8-bit input-output port. Each bit can be assigned to be an input or an output. TxD: Serial port transmitter data output pin. RxD: Serial port receiver data input pin with high impedance. $\overline{\text{INT}}$: Interrupt Request Input pin. TM0IO-TM1IO: One of the following signals is output or input. <ul style="list-style-type: none"> • Clock at twice the frequency range of the 16-bit timer overflow • Load trigger signal to the capture register input • Setting value output Whether the signal is input or output depends on the mode.
P4.0/TM0CK P4.1/TM1CK P4.2/PWM0 P4.3/PWM1 P4.4 – P4.7/ TRANS0 – 3	I/O	P4: 8-bit input-output port. Each bit can be assigned to an input or an output. TM0CK, TM1CK: Clock input pins of timer 0, timer 1. TRANS: The input pins which sense the rising edge and set the flag. PWM: 12-bit pulse-width modulator output pin.
P5.0 – P5.7/ AI0 –AI7	I	P5: 8-bit input port. AI: Analog signal input pin for A/D converter.

PIN DESCRIPTIONS (Continued)

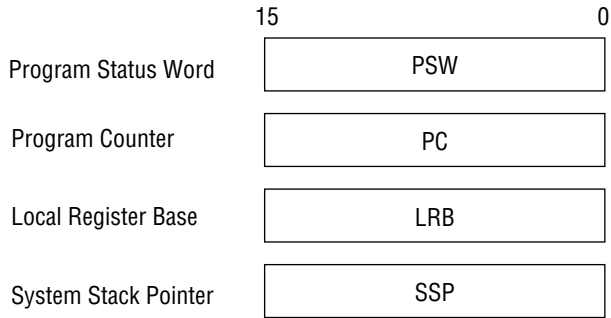
Symbol	Type	Description
RESOUT	0	Outputs 'H' level when the CPU is in RESET status. Reset to 'L' level in some programs.
ALE	0	Address Latch Enable: The timing pulse to latch the lower 8 bits of the address output from port 0 when the CPU accesses the external memory.
$\overline{\text{PSEN}}$	0	Program Store Enable: The strobe pulse to fetch to external program memory.
$\overline{\text{RD}}$	0	Output strobe activated during a bus read cycle. Used to enable data on to the bus from the external data memory.
$\overline{\text{WR}}$	0	Output strobe during a bus write cycle. Used as write strobe to external data memory.
READY	I	Used when the CPU accesses low speed peripherals.
$\overline{\text{EA}}$	I	Normally set to 'H' level. If set to 'L' level, the CPU fetches the code from external program memory.
$\overline{\text{FLT}}$	I	If $\overline{\text{FLT}}$ is 'H' level, ALE, $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{PSEN}}$ are set to 'H' level when reset. If $\overline{\text{FLT}}$ is set to 'L', ALE, $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{PSEN}}$ are set to floating level when reset.
$\overline{\text{RES}}$	I	RESET input pin.
OSCO	I	Clock oscillation pins
OSC1	0	
$\overline{\text{NMI}}$	I	Nonmaskable interrupt input pin (falling edge)
V _{REF}	I	Reference voltage input pin for A/D converter.
AGND	I	Ground for A/D converter.
V _{DD}	I	System power supply.
GND	I	Ground.

REGISTERS

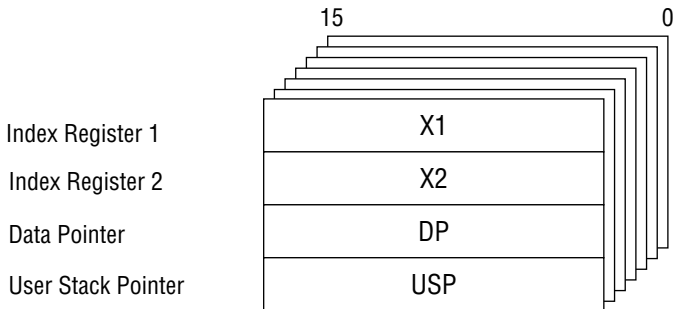
Accumulator



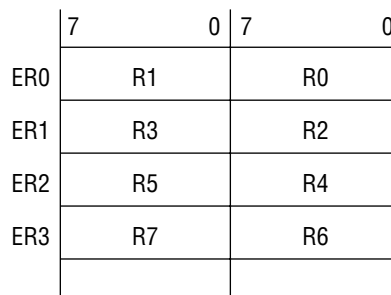
Control Register (CR)



Pointing Register (PR)



Local Register



SFR

Address (HEX)	Name	Symbol	R/W	8/16-bit Operation	Reset				
0000	System stack pointer	SSP	R/W	8/16	FFH				
0001		(ASSP)			FFH				
0002	Local register base	LRB			8	8	undefined		
0003		(ALRB)					undefined		
0004☆	Program status word	PSWL (APSW)					R/W	8	C8H
0005☆		PSWH							0CH
0006	Accumulator	ACC							R/W
0007		ACC	00H						
0010☆	Standby control register	SBYCON	W	8					
0011	Watchdog timer	WDT			00H/WDT is stopped				
0012☆	Peripheral control register	PRPHF			R/W	FDH			
0013	Stop code acceptor	STPACP	W	8	"0"				
0018☆	Interrupt request register	IRQ	R/W	8/16	08H				
0019☆					0FH				
001A☆	Interrupt enable register	IE			8	08H			
001B☆						0FH			
001C☆	External linterrupt control register	EXICON		R/W		8	FCH		
0020	Port 0 data register	P0					undefined		
0021	Port 0 mode register	P0IO			00H				
0022	Port 1 data register	P1	undefined						
0023	Port 1 mode register	P1IO	00H						
0024	Port 2 data register	P2	undefined						
0025	Port 2 mode register	P2IO	00H						
0026☆	Port 2 secondary function control register	P2SF	C7H						
0028	Port 3 data register	P3	undefined						
0029	Port 3 mode register	P3IO	00H						
002A☆	Port 3 secondary function control register	P3SF	C0H						
002C	Port 4 data register	P4	undefined						
002D	Port 4 mode register	P4IO	00H						
002E	Port 4 secondary function control register	P4SF	00H						
002F	Port 5	P5	R	—					
0030	Timer 0 counter	TM0	R/W	16	00H				
0031					00H				
0032	Timer 0 register	TMR0			00H				
0033					00H				
0034	Timer 1 counter	TM1			00H				
0035					00H				
0036	Timer 1 register	TMR1			00H				
0037			00H						

☆ indicates that the register has a nonexistent bit.

SFR (Continued)

Address (HEX)	Name	Symbol	R/W	8/16-bit Operation	Reset	
0040	Timer 0 control register	TCON0	R/W	8	00H	
0041	Timer 1 control register	TCON1			00H	
0046☆	Transition detector register	TRANSIT			undefined	
0048	Serial port transmission baud rate generator counter	STTM			00H	
0049	Serial port transmission baud rate generator register	STTMR			00H	
004A☆	Serial port transmission baud rate generator control register	STTMC			0FH	
0050☆	Serial port transmission mode control register	STCON	W	8	82H	
0051	Serial port transmission data buffer register	STBUF			undefined	
0054	Serial port receiving mode control register	SRCON	R/W	8/16	12H	
0055	Serial port receiving data buffer register	SRBUF	R		undefined	
0056☆	Serial port receiving error register	SRSTAT	R/W		FOH	
0058☆	A/D scan mode register	ADSCAN			80H	
0060☆ 0061	A/D conversion result register 0	ADCR0	R		8/16	undefined
0062☆ 0063	A/D conversion result register 1	ADCR1				
0064☆ 0065	A/D conversion result register 2	ADCR2				
0066☆ 0067	A/D conversion result register 3	ADCR3				
0068☆ 0069	A/D conversion result register 4	ADCR4				
006A☆ 006B	A/D conversion result register 5	ADCR5				
006C☆ 006D	A/D conversion result register 6	ADCR6				
006E☆ 006F	A/D conversion result register 7	ADCR7				

☆ indicates that the register has a nonexistent bit.

SFR (Continued)

Address (HEX)	Name	Symbol	R/W	8/16-bit operation	Reset
0070	PWM 0 counter	PWMC0	R/W	8/16	00H
0071☆					FOH
0072	PWM 0 register	PWMR0			00H
0073☆					FOH
0074	PWM 1 counter	PWMC1			00H
0075☆					FOH
0076	PWM 1 register	PWMR1			00H
0077☆					FOH
0078☆	PWM 0 control register	PWCON0		8	0CH
007A☆	PWM 1 control register	PWCON1			0CH

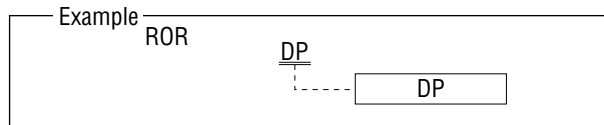
☆ indicates that the register has a nonexistent bit.

ADDRESSING MODES

The MSM66101 provides independent 64K-byte data and 64K-byte program spaces with various types of addressing modes. These modes are shown below, for both RAM (for data space) and ROM (for program space).

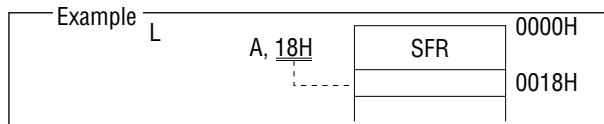
1. RAM Addressing Mode (for data space)

1.1 Register Direct Addressing

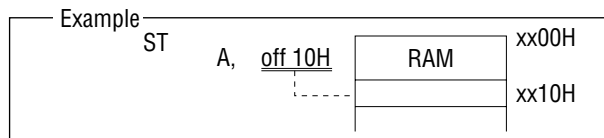


1.2 Page Addressing

a) Zero Page

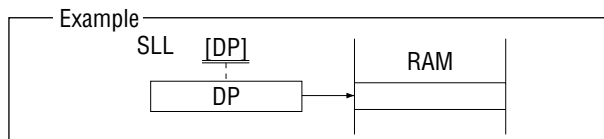


b) Direct Page

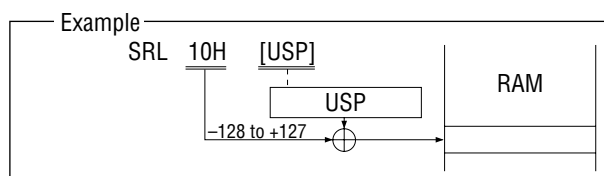


1.3 Pointing Register (PR) Indirect Addressing

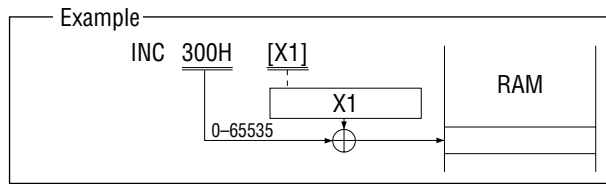
a) Data Point (DP) Indirect



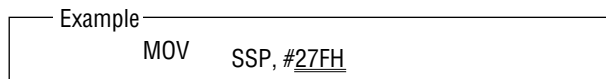
b) User Stack Pointer (USP) Indirect



c) Index Register (X1, X2) Indirect

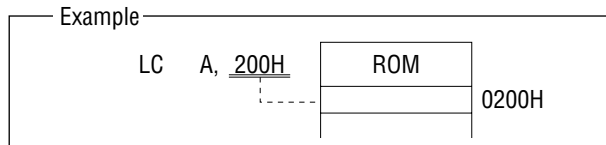


1.4 Immediate Addressing

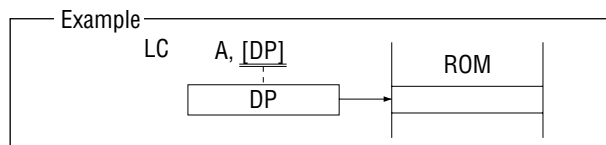


2. ROM Addressing Mode (for program space)

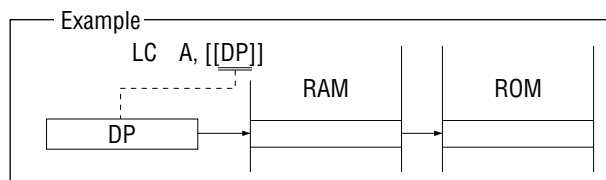
2.1 Direct Addressing



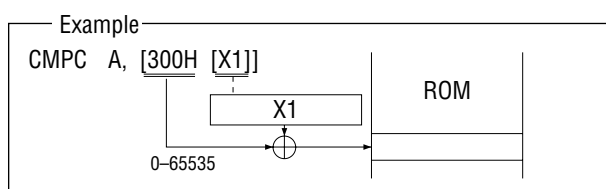
2.2 Simple Indirect Addressing



2.3 Double Indirect Addressing

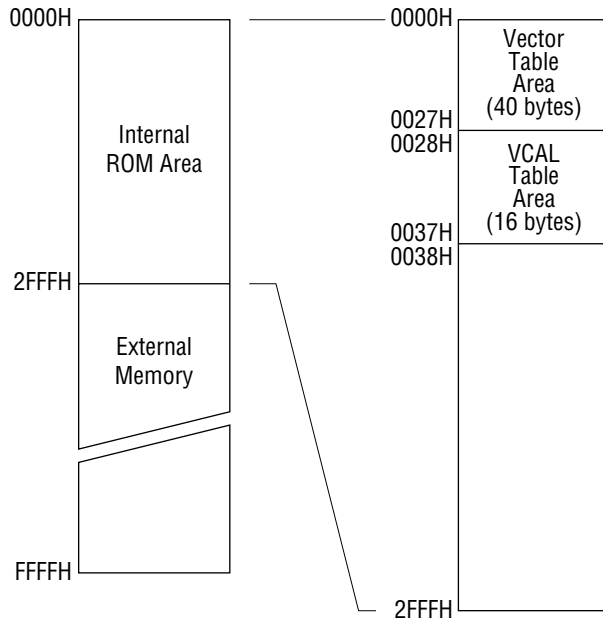


2.4 Indirect Addressing with 16-bit Offset

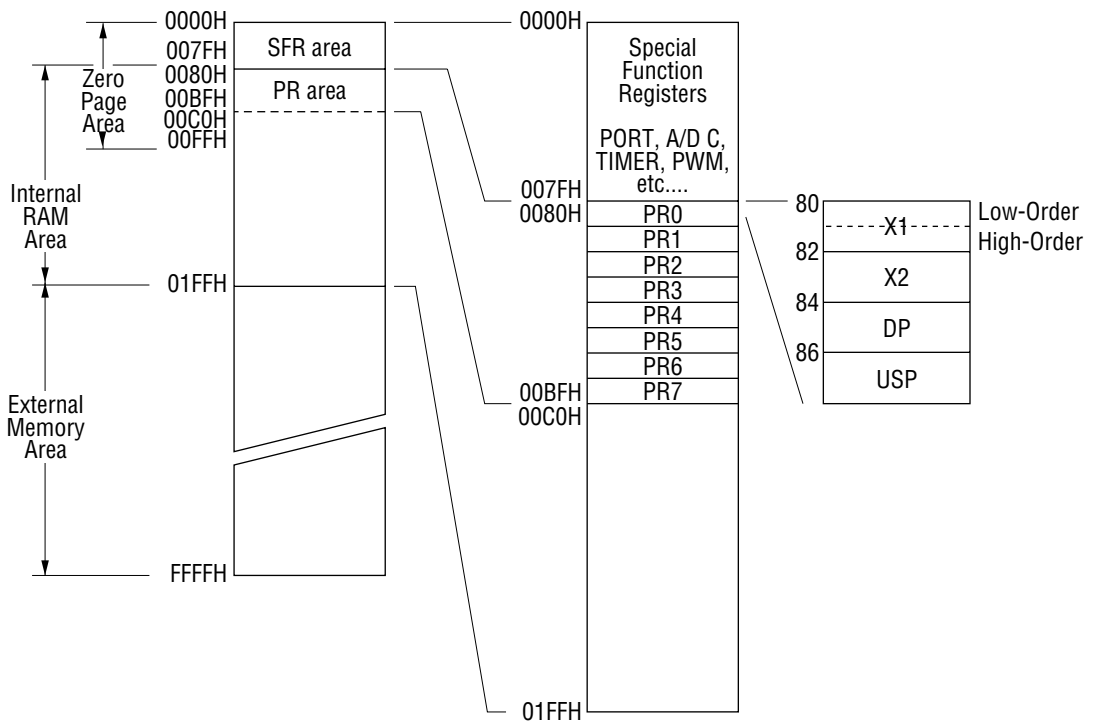


MEMORY MAPS

Program Memory Space



Data Memory Space



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Parameter	Symbol	Condition	Rating	Unit	
Supply Voltage	V _{DD}	GND = AGND = 0V	-0.3 to 7.0	V	
Input Voltage	V _I		-0.3 to V _{DD} +0.3		
Output Voltage	V _O		-0.3 to V _{DD} +0.3		
Analog Ref. Voltage	V _{REF}		-0.3 to V _{DD} +0.3		
Analog Input Voltage	V _{AI}		-0.3 to V _{REF}		
Power Dissipation	P _D	Ta=85°C per package	64-pin shrink DIP	930	mW
			64-pin QFP	565	
			68-pin QFJ	1120	
		Ta = 85°C per output	50		
Storage Temperature	T _{STG}	—	-55 to +150	°C	

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit	
Supply Voltage	V _{DD}	f _{OSC} ≤ 10MHz	4.5 to 5.5	V	
Memory Hold Voltage	V _{DDH}	f _{OSC} = 0Hz	2.0 to 5.5		
Operating Frequency	f _{OSC}	V _{DD} = 5V ±10%	0 to 10	MHz	
Ambient Temperature	Ta	—	-40 to +85	°C	
Fan Out	N	MOS load	20	—	
		TTL load	P0		2
			P1, P2, P3, P4		1

ELECTRICAL CHARACTERISTICS

DC Characteristics

($V_{DD} = 5V \pm 10\%$, $T_a = -40$ to $+85^\circ C$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1, 3, 6	V_{IH}	—	2.4	—	$V_{DD}+0.3$	V
"H" Input Voltage 5, 7			4.0	—	$V_{DD}+0.3$	
"H" Input Voltage 8			4.2	—	$V_{DD}+0.3$	
"H" Input Voltage 2			3.6	—	$V_{DD}+0.3$	
"L" Input Voltage 1, 2, 3, 6	V_{IL}	—	-0.3	—	0.8	
"L" Input Voltage 5, 7			-0.3	—	0.8	
"L" Input Voltage 8			-0.3	—	0.4	
"H" Output Voltage 1, 4	V_{OH}	$I_O = -400\mu A$	4.2	—	—	
"H" Output Voltage 2		$I_O = -200\mu A$	4.2	—	—	
"L" Output Voltage 1, 4	V_{OL}	$I_O = 3.2mA$	—	—	0.4	
"L" Output Voltage 2		$I_O = 1.6mA$	—	—	0.4	
Input Leakage Current 3, 6, 7	I_{IH}/I_{IL}	$V_I = V_{DD}/0V$	—	—	1/-1	μA
Input Current 5			—	—	1/-20	
Input Current 8			—	—	10/-10	
"H" Output Current 1	I_{OH}	$V_O = 2.4V$	-2	—	—	mA
"H" Output Current 2			-1	—	—	
"L" Output Current 1	I_{OL}		10	—	—	
"L" Output Current 2			5	—	—	
Output Leakage Current 1, 2, 4	I_{LO}	$V_O = V_{DD}/0V$	—	—	± 2	μA
Input Capacitance	C_I	$f = 1MHz$	—	5	—	pF
Output Capacitance	C_O	$T_a = 25^\circ C$	—	7	—	
Analog Reference Power Supply Current	I_{REF}	A/D in operation	—	0.3	2	mA
		A/D stopped	—	0.5	10	μA
Current Consumption (during STOP) *	I_{DDS}	$V_{DD} = 2V$	—	0.2	10	μA
		—	—	1	100	
Current Consumption (during HALT)	I_{DDH}	$f_{OSC} = 10MHz$ No load	—	6	10	mA
Current Consumption	I_{DD}		—	20	35	

1 : Applied to P0

2 : Applied to P1, P2,P3 and P4

3 : Applied to P5

4 : Applied to ALE, \overline{PSEN} , \overline{RD} , \overline{WR} and RESOUT

5 : Applied to \overline{RES} and \overline{NMI}

6 : Applied to READY and \overline{EA}

7 : Applied to \overline{FLT}

8 : Applied to OSC0

* : V_{DD} or GND for ports serving as the input pin. No-load for any other.

AC Characteristics

• **External program memory control**

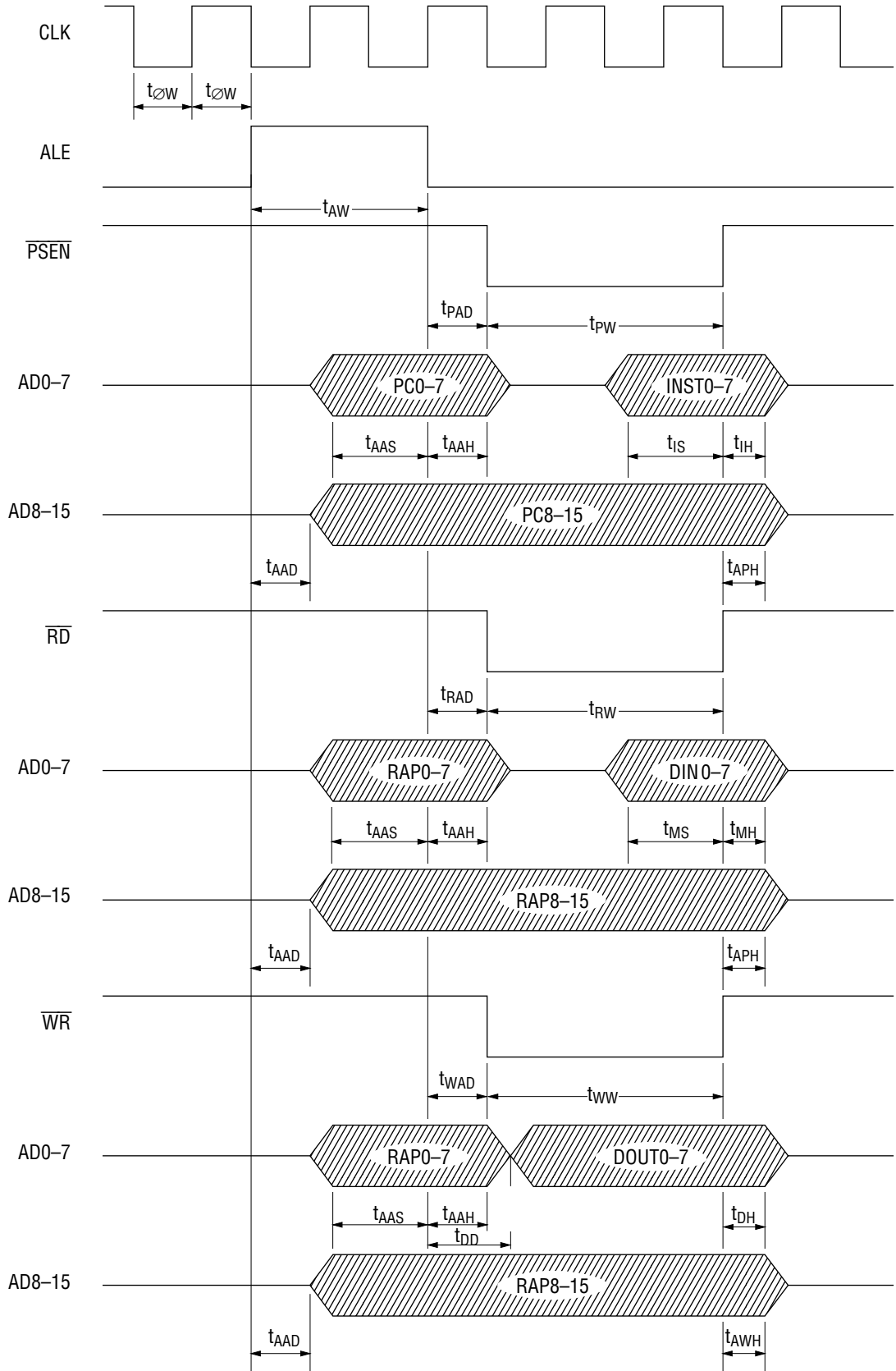
($V_{DD}=5V\pm 10\%$, $T_a=-40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock (OSC) Pulse	$t_{\phi W}$	—	50	—	ns
ALE Pulse Width	t_{AW}	$C_L = 50\text{pF}$	$3t_{\phi W}-20$	—	
$\overline{\text{PSEN}}$ Pulse Width	t_{PW}		$4t_{\phi W}-20$	—	
$\overline{\text{PSEN}}$ Pulse Delay Time	t_{PAD}		$t_{\phi W}-20$	$t_{\phi W}+20$	
Low Address Setup time	t_{AAS}		$2t_{\phi W}-35$	$2t_{\phi W}+20$	
Low Address Hold Time	t_{AAH}		$t_{\phi W}-20$	$t_{\phi W}+40$	
High Address Delay Time	t_{AAD}		$t_{\phi W}-20$	$t_{\phi W}+40$	
High Address Hold Time	t_{APH}		$t_{\phi W}-20$	$t_{\phi W}+40$	
Instruction Setup Time	t_{IS}		100	—	
Instruction Hold Time	t_{IH}		0	$t_{\phi W}-20$	

• **External data memory control**

($V_{DD}=5V\pm 10\%$, $T_a=-40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock (OSC) Pulse	$t_{\phi W}$	—	50	—	ns
ALE Pulse Width	t_{AW}	$C_L = 50\text{pF}$	$3t_{\phi W}-20$	—	
$\overline{\text{RD}}$ Pulse Width	t_{RW}		$4t_{\phi W}-20$	—	
$\overline{\text{WR}}$ Pulse Width	t_{WW}		$4t_{\phi W}-20$	—	
$\overline{\text{RD}}$ Pulse Delay Time	t_{RAD}		$t_{\phi W}-20$	$t_{\phi W}+20$	
$\overline{\text{WR}}$ Pulse Delay Time	t_{WAD}		$t_{\phi W}-20$	$t_{\phi W}+20$	
Low Address Setup Time	t_{AAS}		$2t_{\phi W}-35$	$2t_{\phi W}+20$	
Low Address Hold Time	t_{AAH}		$t_{\phi W}-20$	$t_{\phi W}+40$	
High Address Setup Time	t_{AAD}		$t_{\phi W}-20$	$t_{\phi W}+40$	
High Address Hold Time	t_{ARH}		$t_{\phi W}-20$	$t_{\phi W}+40$	
High Address Hold Time	t_{AWH}		$t_{\phi W}-20$	$t_{\phi W}+40$	
Memory Data Setup Time	t_{MS}		100	—	
Memory Data Hold Time	t_{MH}		0	$t_{\phi W}-20$	
Data Delay Time	t_{DD}		$t_{\phi W}-20$	$t_{\phi W}+40$	
Data Hold Time	t_{DH}		$t_{\phi W}-20$	$t_{\phi W}+40$	



• Serial port control

Master mode

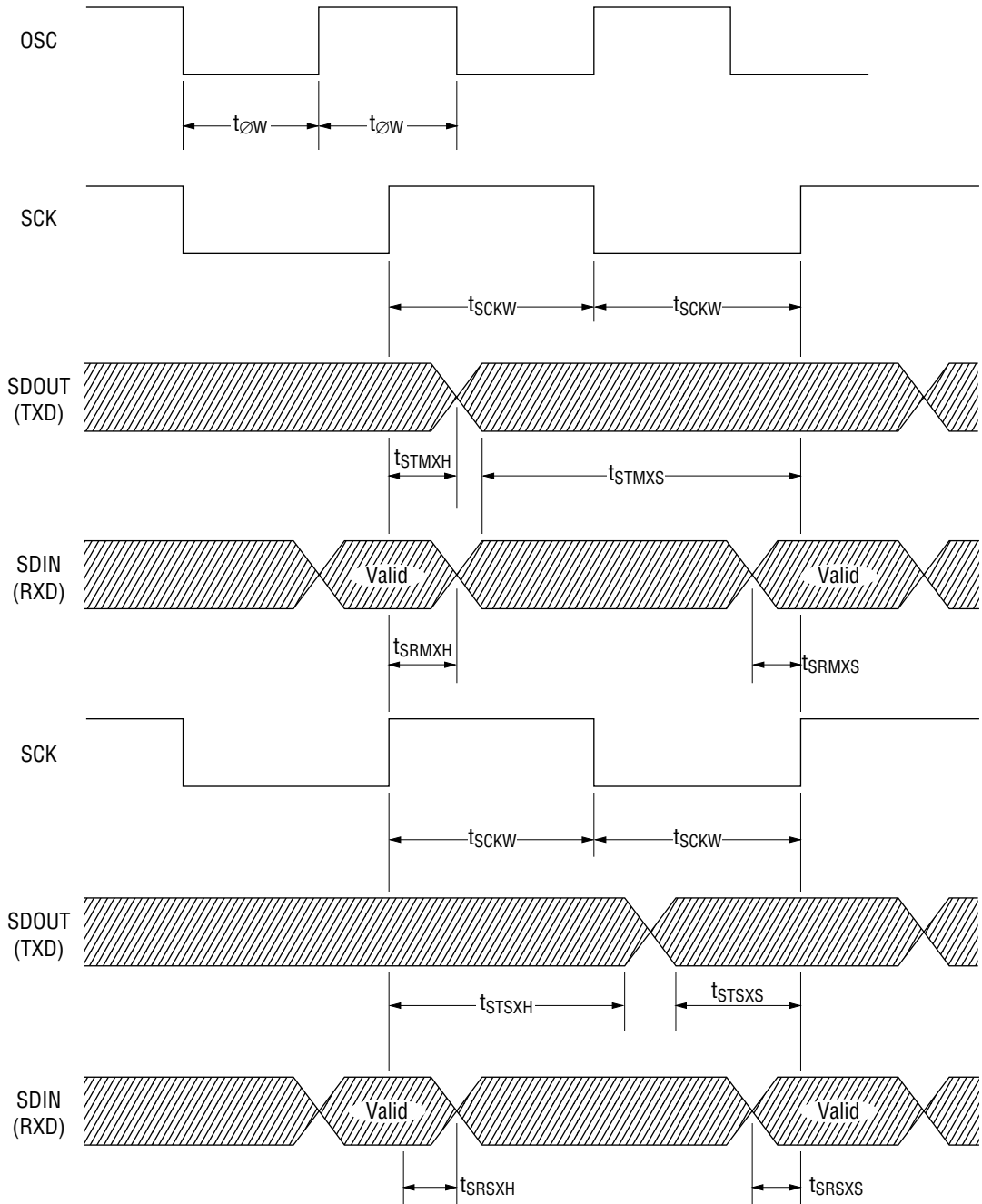
($V_{DD}=5V\pm 10\%$, $T_a=-40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock (OSC) Pulse Width	$t_{\phi W}$	—	50	—	ns
Serial Clock Pulse Width	t_{SCKW}	—	$8t_{\phi W}$	—	
Output Data Setup Time	t_{STMXS}	$C_L=50\text{pF}$	$8t_{\phi W}+40$	—	
Output Data Hold Time	t_{STMXH}		$6t_{\phi W}-20$	—	
Input Data Setup Time	t_{SRMXS}		$2t_{\phi W}+10$	—	
Input Data Hold Time	t_{SRMXH}		50	—	

Slave mode

($V_{DD}=5V\pm 10\%$, $T_a=-40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock (OSC) Pulse Width	$t_{\phi W}$	—	50	—	ns
Serial Clock Pulse Width	t_{SCKW}	—	$8t_{\phi W}$	—	
Output Data Setup Time	t_{STSXS}	$C_L=50\text{pF}$	$6t_{\phi W}+40$	—	
Output Data Hold Time	t_{STSXH}		$6t_{\phi W}-20$	—	
Input Data Setup Time	t_{SRSXS}		100	—	
Input Data Hold Time	t_{SRSXH}		100	—	



A/D Converter Characteristics

• Operating range

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	$f_{OSC} \leq 10\text{MHz}$	4.5	—	5.5	V
Analog Reference Voltage	V_R	$V_{AG} = \text{GND} = 0\text{V}$	4.5	—	V_{DD}	
Analog Input Voltage	V_{AI}		V_{AG}	—	V_R	
Analog Reference Power Voltage Resistance	R_R		—	16	—	k Ω
Operating Temperature	T_{op}	$V_{DD} = 5\text{V} \pm 10\%$	-40	—	+85	$^{\circ}\text{C}$

• A/D Converter accuracy

Normal operation mode

($V_{DD}=5\text{V} \pm 10\%$, $f_{OSC}=10\text{MHz}$, $T_a=-40$ to $+85^{\circ}\text{C}$)

Parameter	Symbol	Condition	Min.		Typ.		Max.		Unit
				*		*		*	
Resolution	n	See the recommended circuit. $V_R=V_{DD}$ $V_{AG}=\text{GND}=0\text{V}$ Analog input source impedance $\leq 5\text{k}\Omega$ One channel conversion time $t_C=64\mu\text{s}$	—	—	—	—	10	10	Bit
Absolute Error	E_A		—	—	—	—	+3.0 -3.5	+2.0 -3.5	LSB
Relative Error	E_R		—	—	—	—	± 1.5	± 1.0	
Zero Point Error	E_Z		0	0	—	—	+3.0	+2.0	
Full Scale Error	E_F		-0.5	-1.0	—	—	-3.5	-3.5	
Differential Linearity Error	E_D		—	—	—	—	+3.0	+2.0	
Crosstalk	E_C		—	—	± 0.5	± 0.5	—	—	

* $V_{DD}=5\text{V}$, $T_a=25^{\circ}\text{C}$

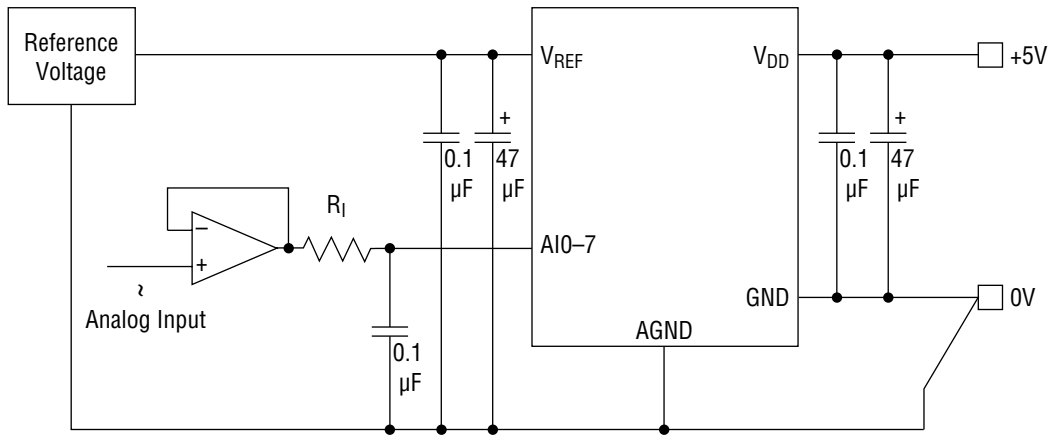
HALT/HOLD operation mode

($V_{DD}=5\text{V} \pm 10\%$, $f_{OSC}=10\text{MHz}$, $T_a=-40$ to $+85^{\circ}\text{C}$)

Parameter	Symbol	Condition	Min.		Typ.		Max.		Unit
				*		*		*	
Resolution	n	See the recommended circuit. $V_R=V_{DD}$ $V_{AG}=\text{GND}=0\text{V}$ Analog input source impedance $\leq 5\text{k}\Omega$ One channel conversion time $t_C=64\mu\text{s}$	—	—	—	—	10	10	Bit
Absolute Error	E_A		—	—	—	—	+2.0 -3.5	+1.0 -2.0	LSB
Relative Error	E_R		—	—	—	—	± 1.0	± 0.5	
Zero Point Error	E_Z		+0.5	+0.5	—	—	+2.0	+1.0	
Full Scale Error	E_F		-1.0	-1.5	—	—	-3.5	-2.0	
Differential Linearity Error	E_D		—	—	—	—	+2.0	+1.0	
Crosstalk	E_C		—	—	± 0.5	± 0.5	—	—	

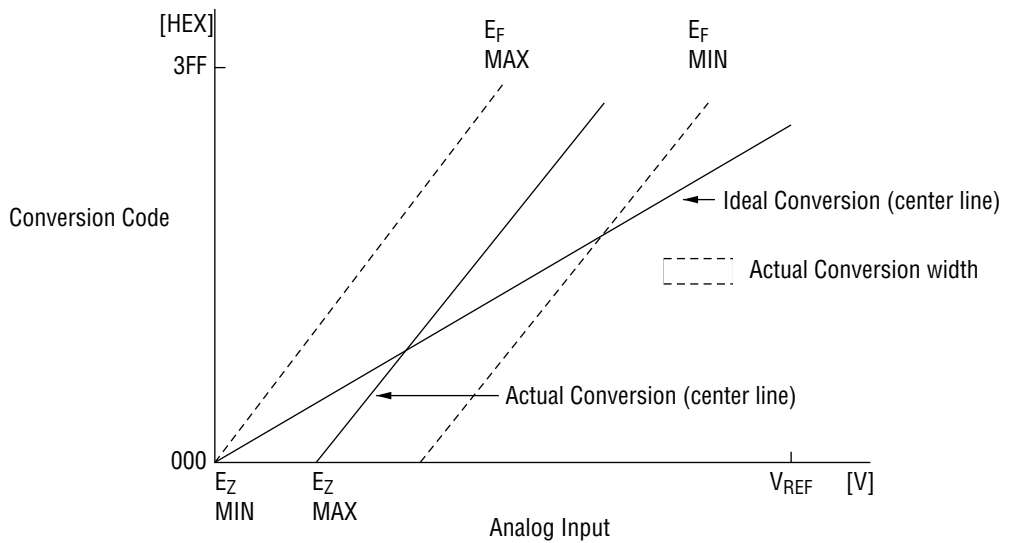
* $V_{DD}=5\text{V}$, $T_a=25^{\circ}\text{C}$

• Recommended circuit



R_1 (Analog input source impedance) $\leq 5k\Omega$

• A/D Converter conversion characteristics 1



Conversion Characteristics Diagram 1

Absolute error (E_A)

The absolute error indicates a difference between actual conversion and ideal conversion, excluding a quantizing error. The absolute error of the A/D converter gets larger as it approaches the zero point or full scale. (See to Conversion Characteristics Diagram 1.)

Relative error (E_R)

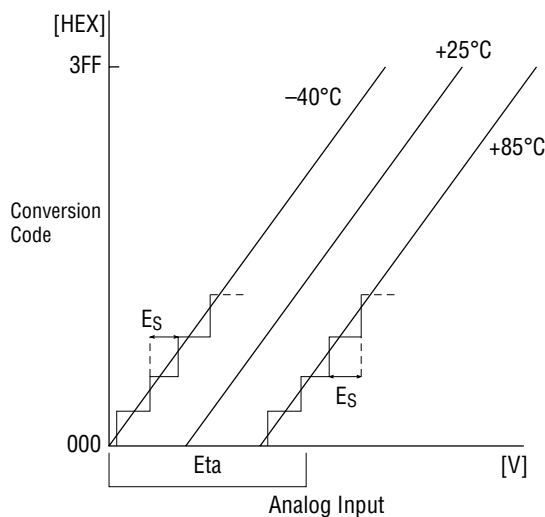
The relative error indicates a deviation from a line which connects the center point of the zero point conversion width with that of the full scale conversion width, excluding a quantizing error.

The relative error of this A/D converter is almost due to a differential linearity error.

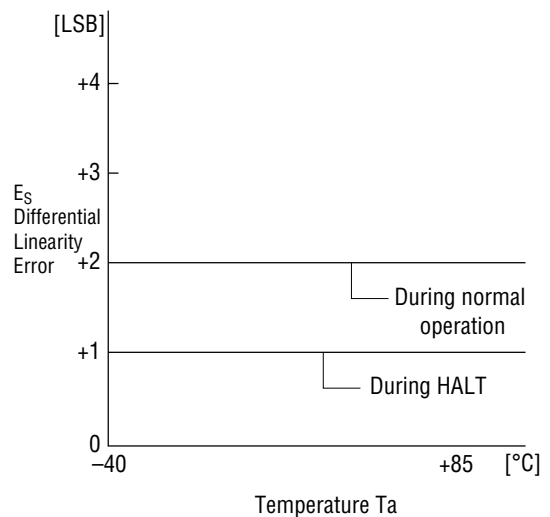
Zero point error (E_Z) and full scale error (E_F)

The zero point error and full scale error indicate a difference between actual conversion and ideal conversion at the zero point and full scale, respectively. (See Conversion Characteristics Diagram 1.)

• A/D Converter conversion characteristics 2 (Temperature Characteristics)



Conversion Characteristics Diagram 2-1



Conversion Characteristics Diagram 2-2

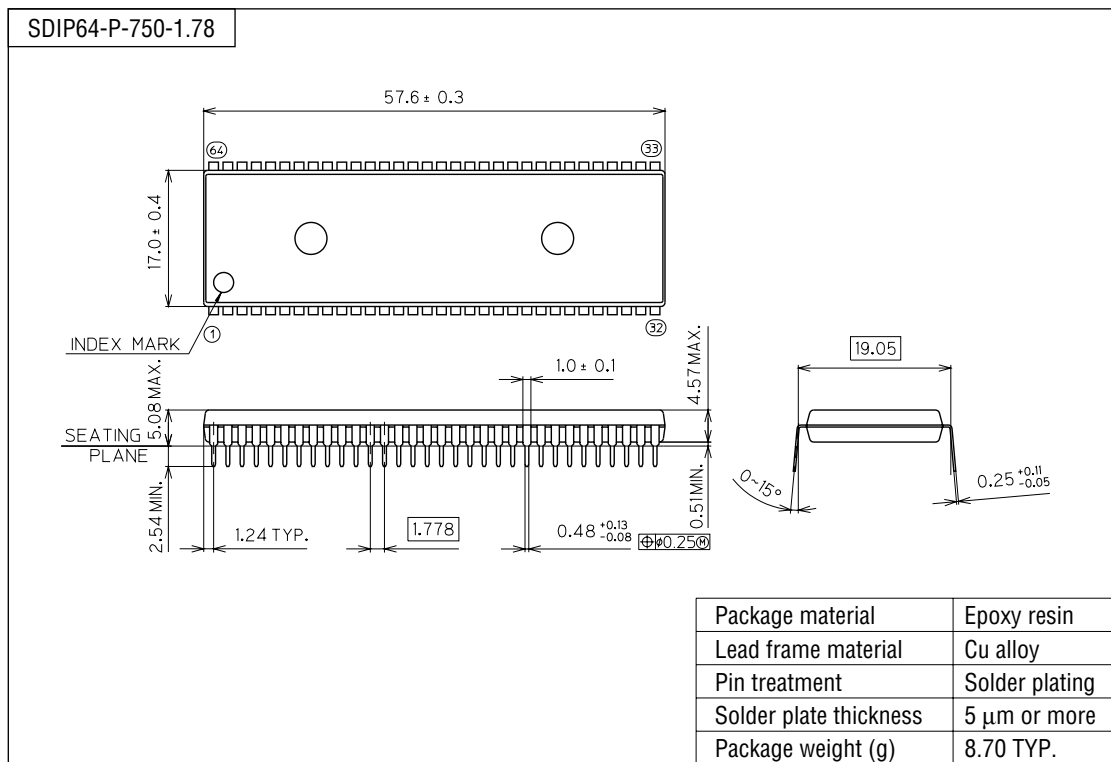
Differential linearity error (E_D)

The differential linearity error indicates a difference between the actual conversion width (actual step width) and ideal value (1LSB).

With this A/D converter, a voltage for actual conversion is shifted and the inclination of a voltage is changed, with changes of temperature (see Conversion Characteristics Diagram 2-1). Specifications described in the foregoing tables are established from Eta shown in Conversion Characteristics Diagram 2-1. Conversion Characteristics Diagram 2-2 shows temperature characteristics of differential linearity error of E_S .

PACKAGE DIMENSIONS

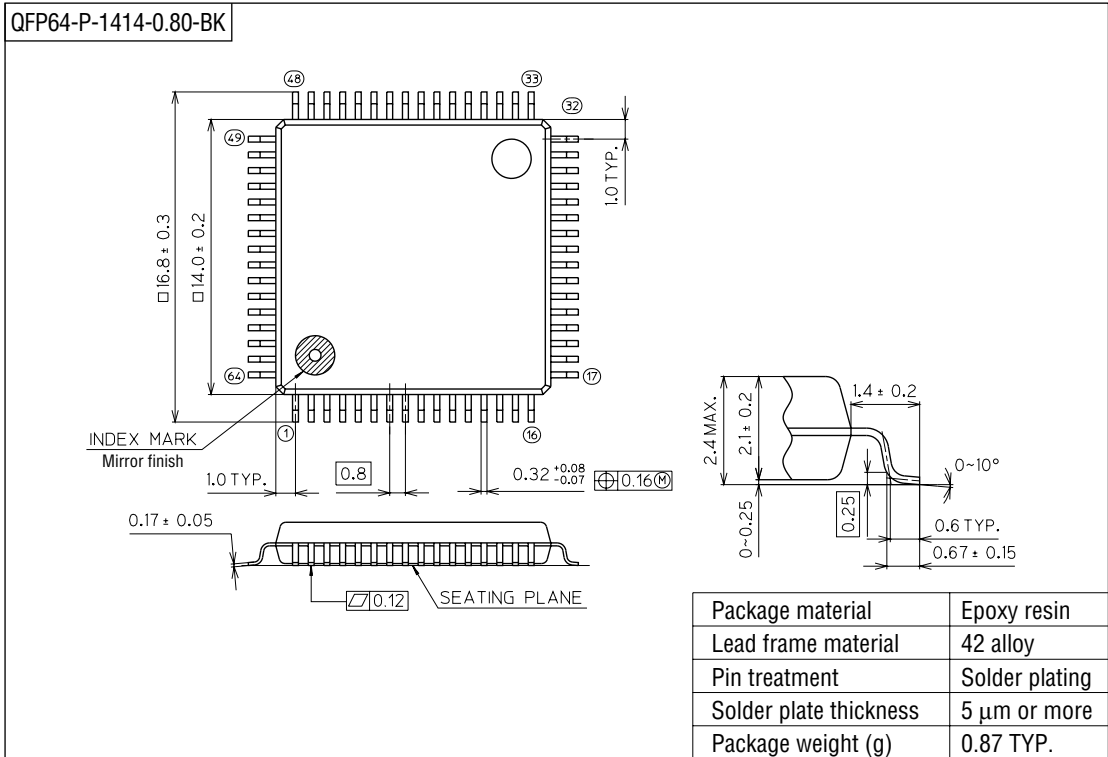
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

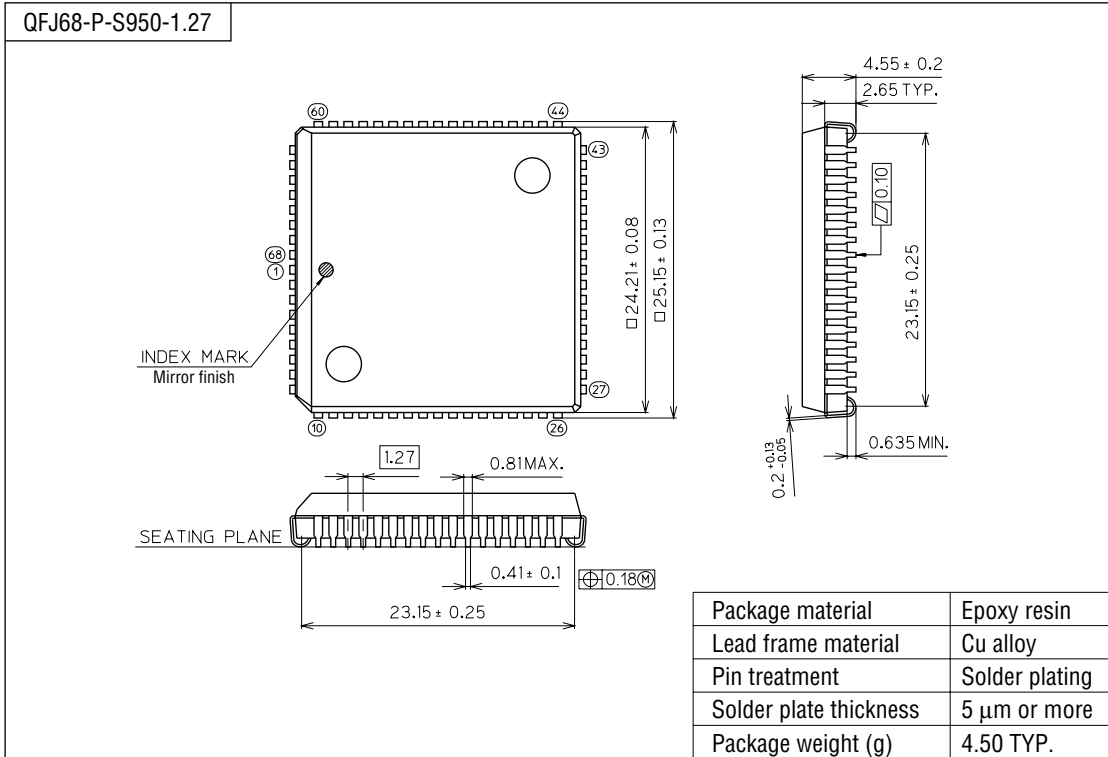
(Unit : mm)



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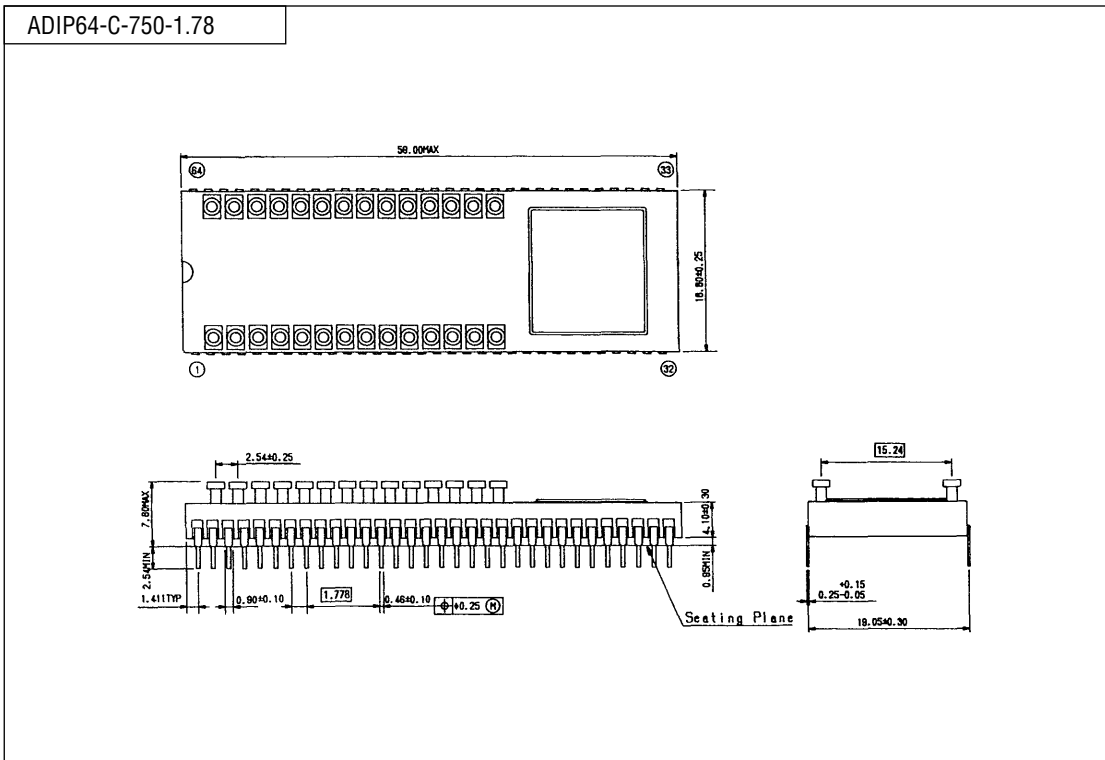
(Unit : mm)



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(Unit : mm)



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